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APPLICANTS

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** CONTINUING DATA *****

This application is a DIV of 10/199,727 07/19/2002 PAT 6,769,103 *BB*

** FOREIGN APPLICATIONS *****

BB

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 05/13/2004

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY CA	SHEETS DRAWING 4	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance	EXAMINER'S SIGNATURE <i>Jonathan Bower</i> Initials <i>BB</i>			
Verified and Acknowledged				

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TITLE

Checking layout accuracy in integrated circuit designs

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